

## REMARKS

This AMENDMENT UNDER 37 CFR 1.111 is filed in reply to the outstanding Office Action of April 24, 2003, and is believed to be fully responsive thereto for reasons set forth below in greater detail.

Initially, the Examiner is thanked for the indication of allowable subject matter in claims 6-12.

Reconsideration is respectfully requested of the rejection of claims 1-5, and 13-20 as being allegedly anticipated by Holst.

The present invention has a major distinction over Holst which provides significant and major advantages of the present invention relative to Holst.

Holst is representative of prior art differential signal sensing schemes which sense a differential signal across two differential sensing wires. This is referred to in the Abstract, lines 2 and 3, "differential signal paths."

This also explained in more detail on column 5, lines 7-25 which explain that "local bit-line pairs" are coupled to each primary sense amplifier 151, which PSAs in turn "supply differential signals on global bit line pairs." In summary, a pair of local bit-lines supply a differential signal to each primary sense amplifier which in turn supplies a differential signal across a pair of lines to a secondary sense amp which in turn supplies a differential signal across a pair of lines to an output. Thus, the signal flow is differential pair to differential pair to differential pair.

This prior art arrangement is referred to in the present specification on page 1 under "Discussion of the Prior Art" as "prior art nondirect sense memory arrays

which include a cross coupled latch.” In fact, Holst shows such a cross coupled latch in Figure 5 formed by the pair of PFET devices P8, P9 and by the pair of NFET devices N5, N4, and also in Figure 4 by the pair of NFET devices N5, N4, and the above located pair of PFET devices (unlabeled).

In contrast to the differential sensing scheme of Holst, the present invention uses a single-ended direct sensing scheme which senses a single signal on a single wire (as opposed to two signals differentially across a pair of wires).

This single-ended sensing scheme is referred to in the present patent application as a “direct sense” memory array or DRAM. See the first paragraph of the SUMMARY OF THE INVENTION which refers to a “direct sense DRAM” and a “single MDQ master data line which carries” an (one) analog level signal to the SSA.”

A “direct sense” single-ended sensing scheme as in the present invention has advantages of providing a much denser memory circuit having only half the sensing signal wires and a much smaller transistor count, which are major advantages relative to a differential sensing scheme as in Holst.

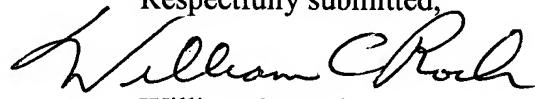
The claims herein have now been amended to clarify the distinctions of the single-ended direct read circuits of the present invention and differential sensing circuits of the prior art such as Holst.

Of course, it should be realized that claim 1 now specifies only a small slice of a memory circuit pursuant to the present invention, which overall comprises many global data lines, but wherein each global data line functions in a manner as specified by claim 1.

It should also be realized that some of the circuits of the present invention (such as the PRIMARY DSA circuits of Figure 1) are coupled to more than one input signal, but those circuits are multiplexed (see more complete circuits of Figures 2 and 5 and explanations) in operation such that only one signal at a time is being processed by the circuit. It is still a direct sense or single-ended circuit, and is not a differential sensing circuit differentially sensing a signal across a pair of input lines as in Holst..

This application is now believed to be in condition for allowance, and a Notice of Allowance is respectfully requested. If the Examiner believes that a telephone conference might expedite prosecution of this case, it is respectfully requested that he call applicant's attorney at (516) 742-4343.

Respectfully submitted,



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